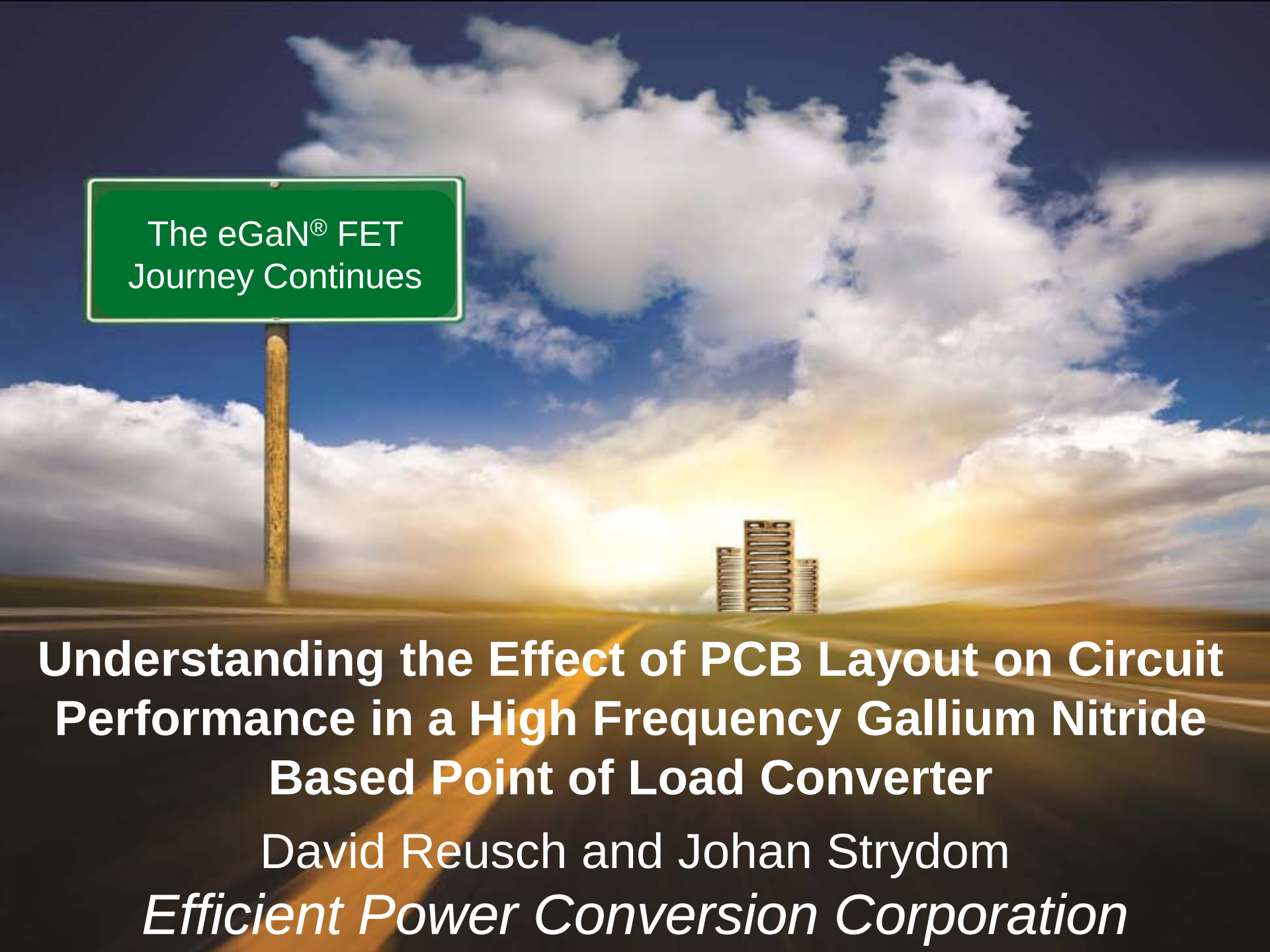


Understanding the Effect of PCB Layout on Circuit Performance in a High Frequency Gallium Nitride Based Point of Load Converter

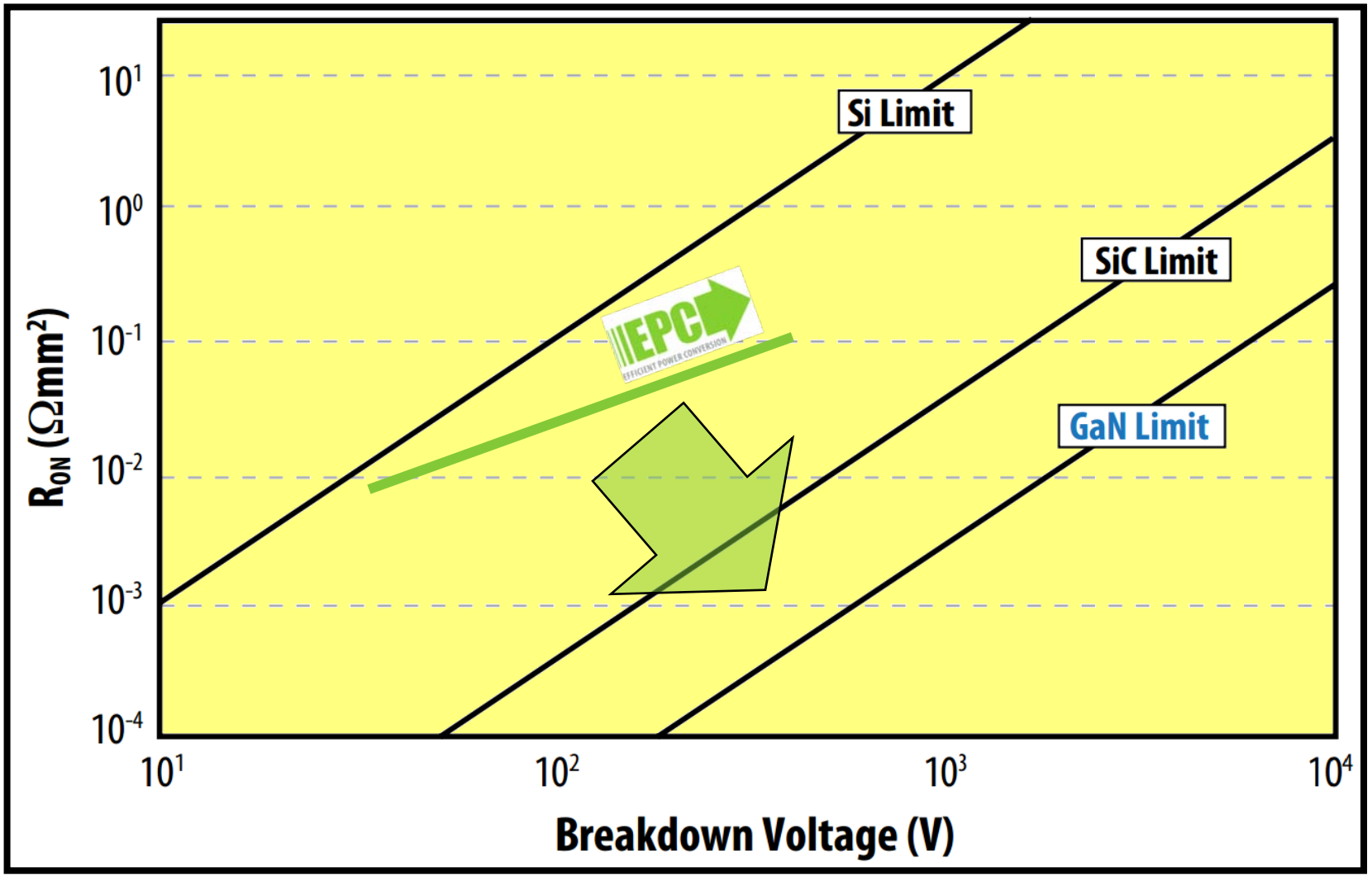
David Reusch and Johan Strydom

Efficient Power Conversion Corporation

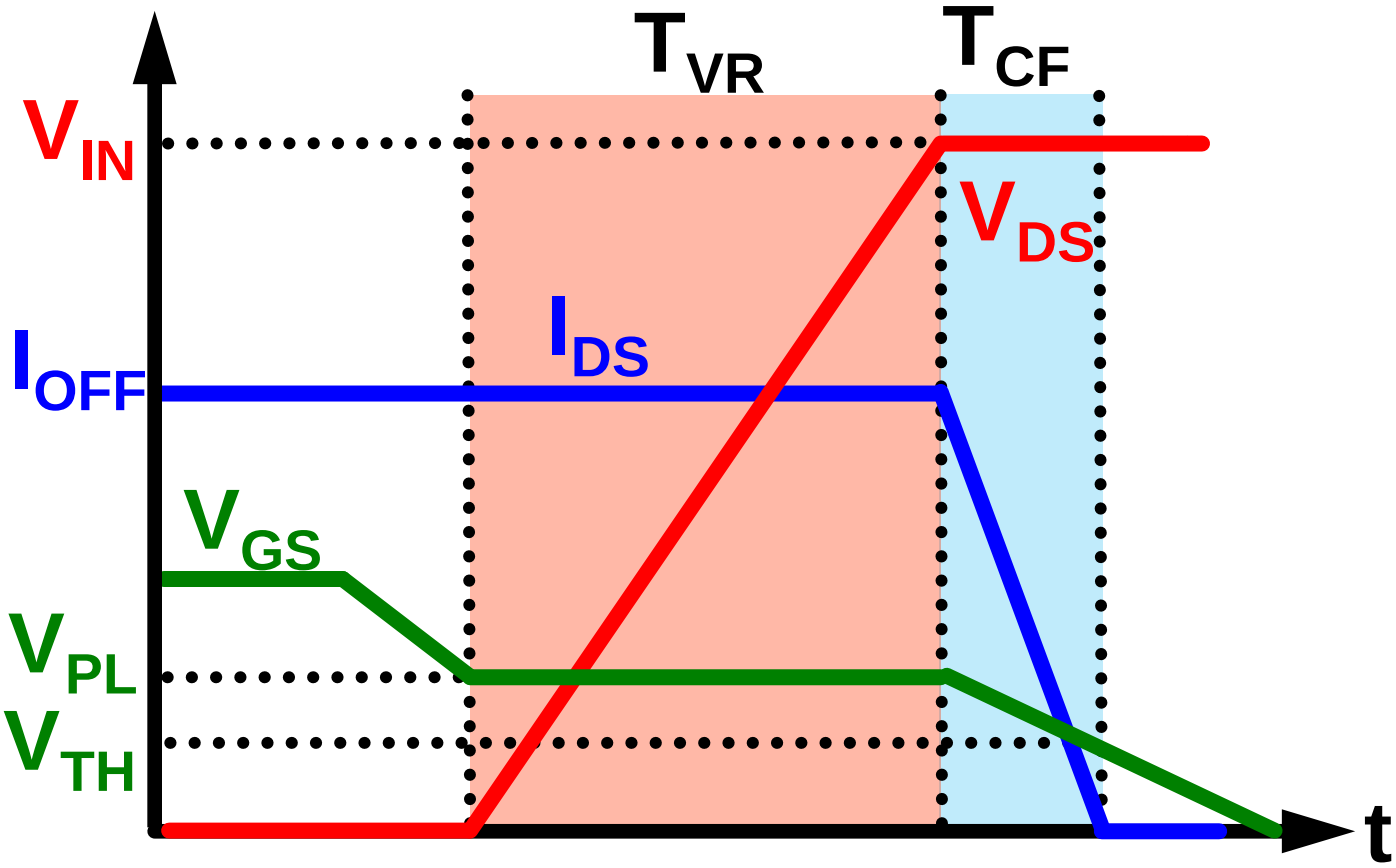
Agenda

- Overview of Current Technology
- Parasitic Impact on Performance
- Conventional Layout Comparison
- Optimal Layout for eGaN® FETs
- Experimental Results
- Summary

Why Gallium Nitride?



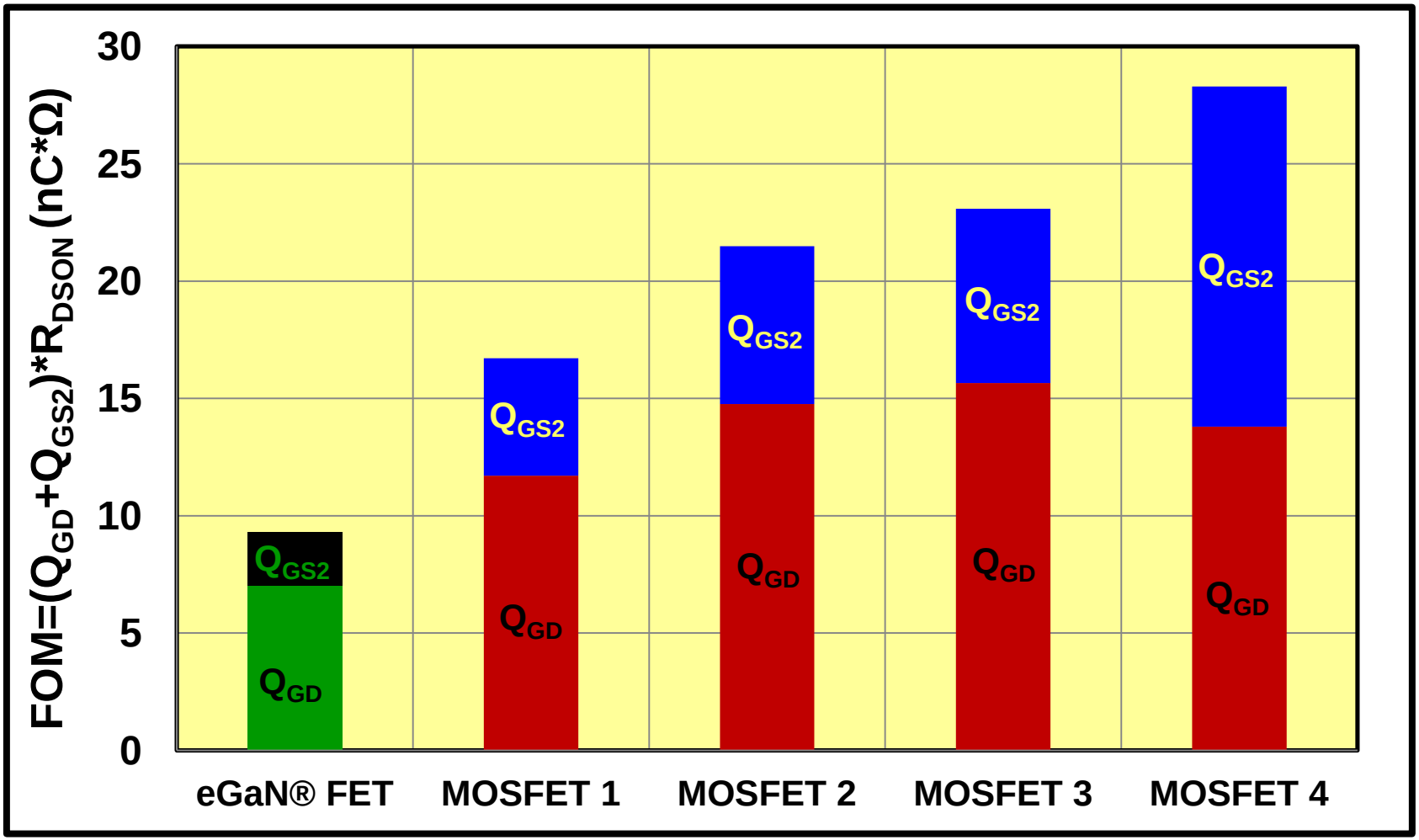
Ideal Hard Switching



$$P_{T_{VR}} \approx \frac{V_{IN} * I_{OFF} * Q_{GD}}{2 * I_G}$$

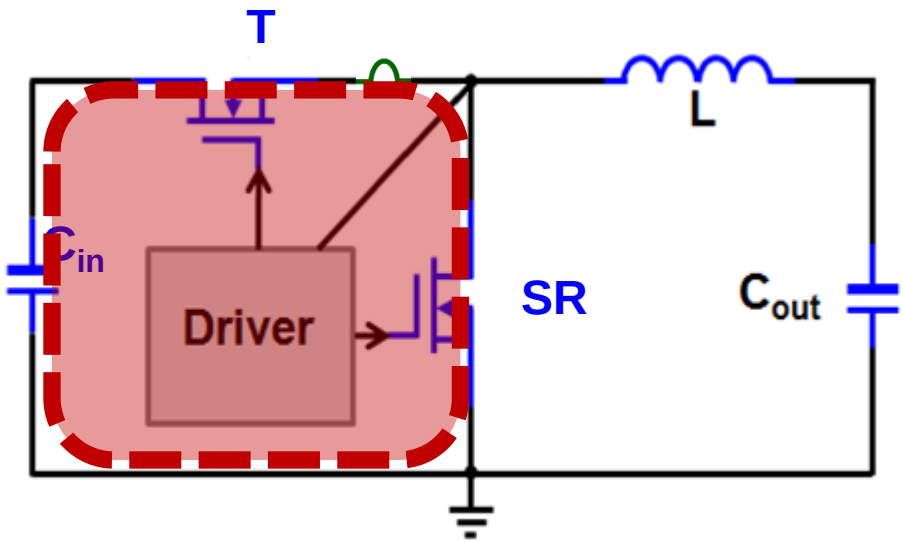
$$P_{T_{CF}} \approx \frac{V_{IN} * I_{OFF} * Q_{GS2}}{2 * I_G}$$

40V Device Comparison



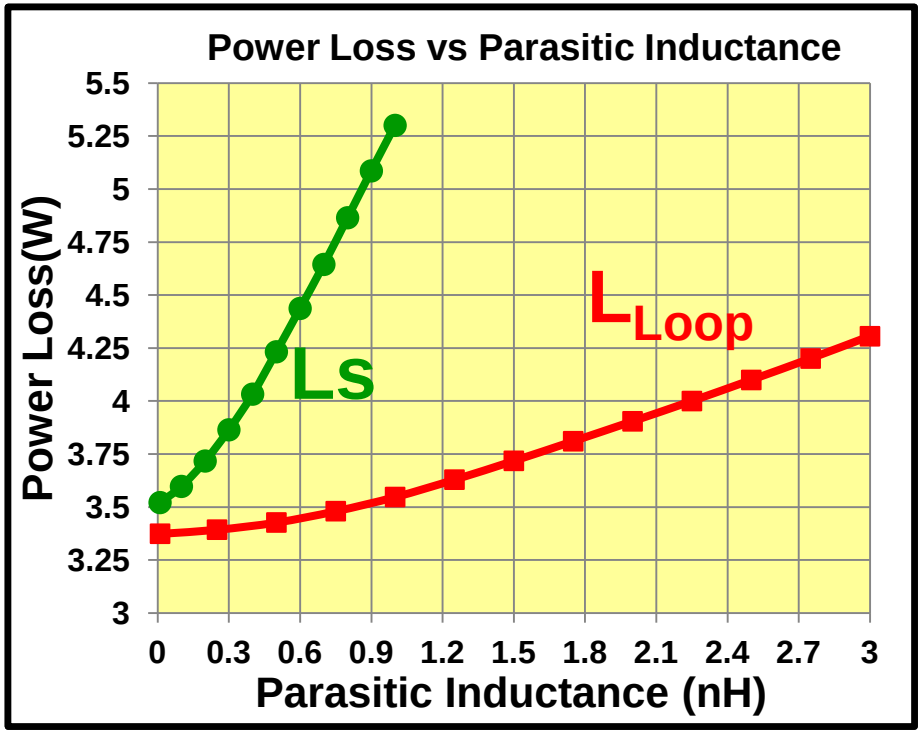
V_{DS}=20 V, I_{DS}= 20 A

Buck Converter Parasitics



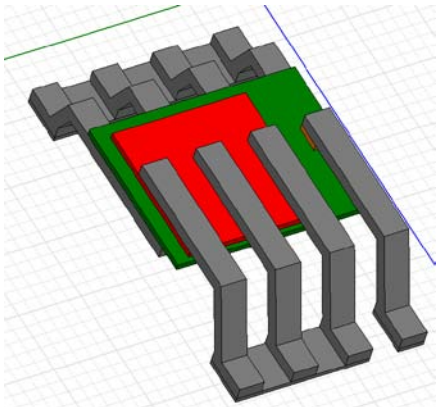
L_S: Common Source Inductance

L_{Loop}: High Frequency Power Loop Inductance

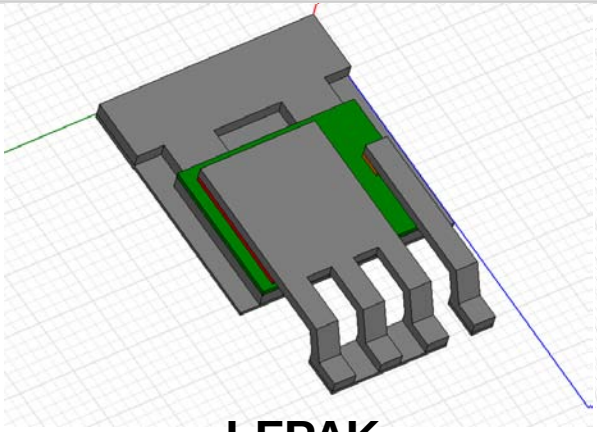


V_{IN}=12 V, V_{OUT}=1.2 V,
F_S=1 MHz, I_{OUT}= 20 A

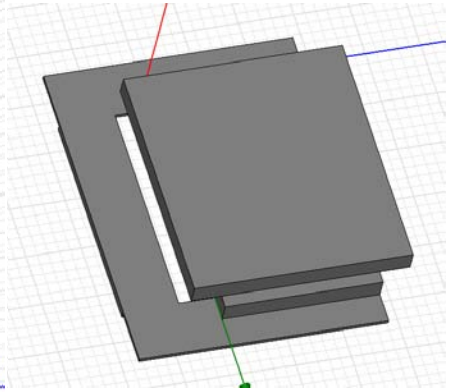
Packaging Evolution



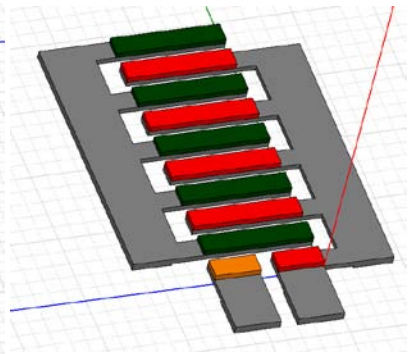
SO-8



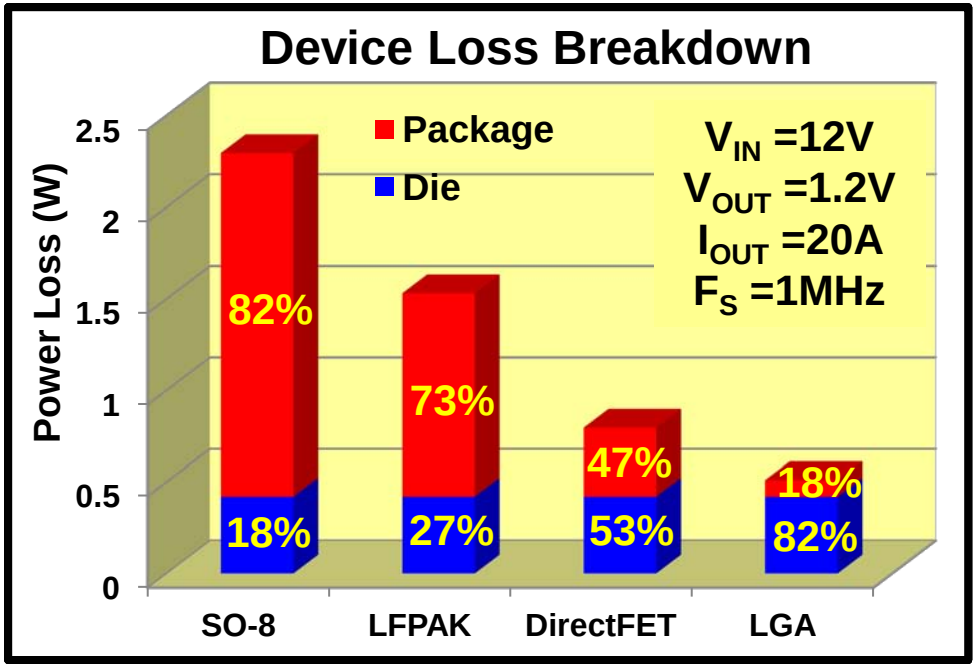
LFPAK

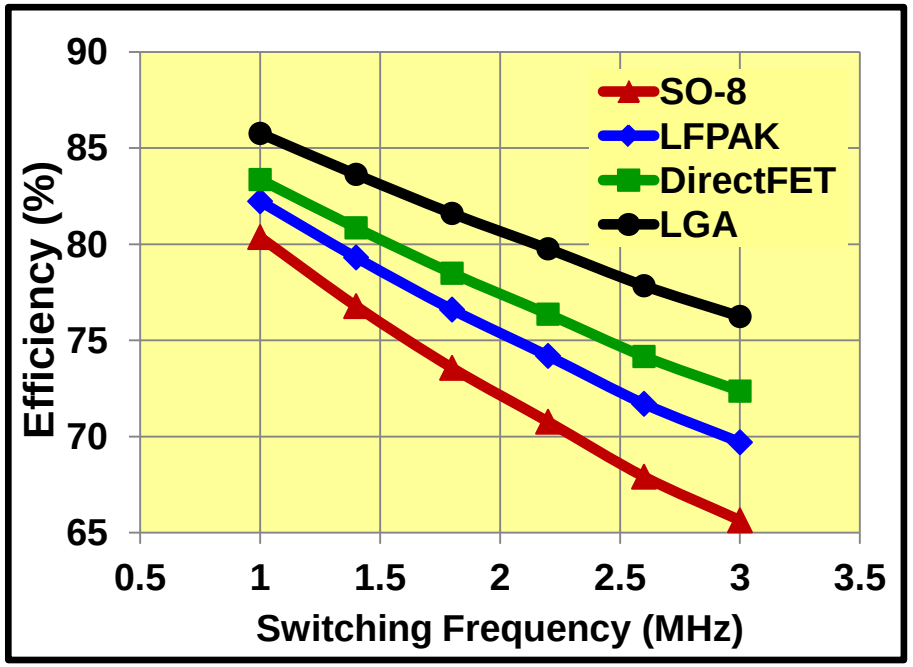


DirectFET



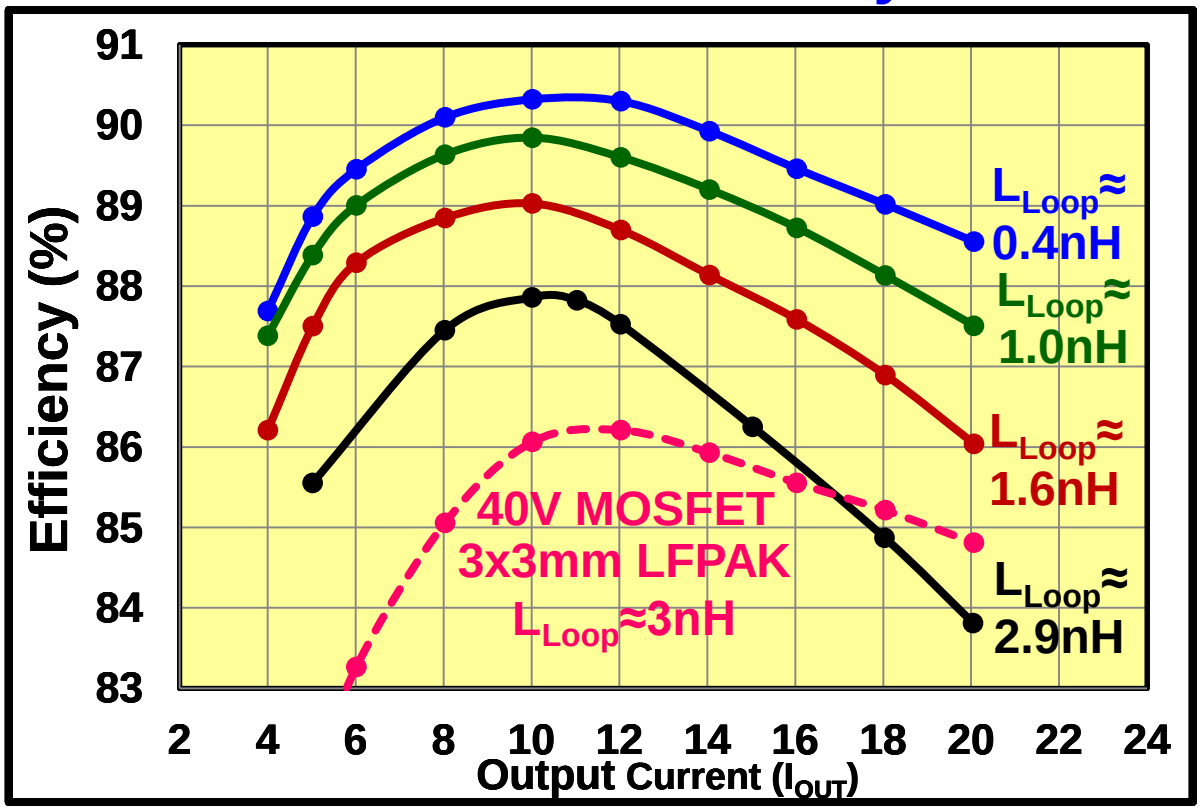
LGA eGaN





Layout Impact on Efficiency

Measured Efficiency



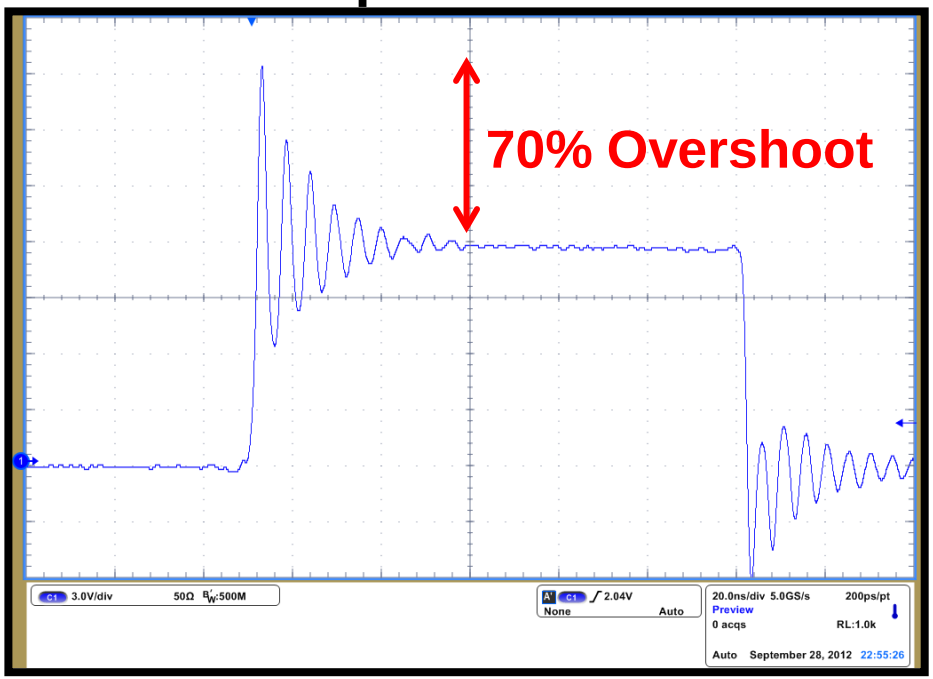
Experimental Prototype

L_{LOOP}≈0.4 nH

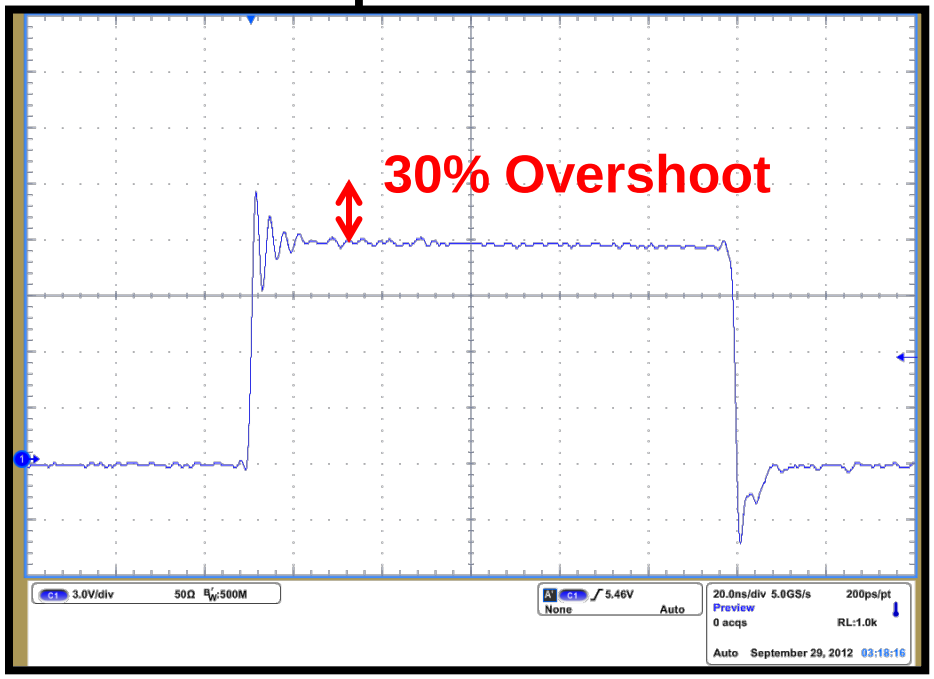
V_{IN}=12 V, V_{OUT}=1.2 V,
F_S=1 MHz, L=150 nH

Layout Impact on Peak Voltage

L_{Loop}≈1.0 nH



L_{Loop} ≈ 0.4 nH



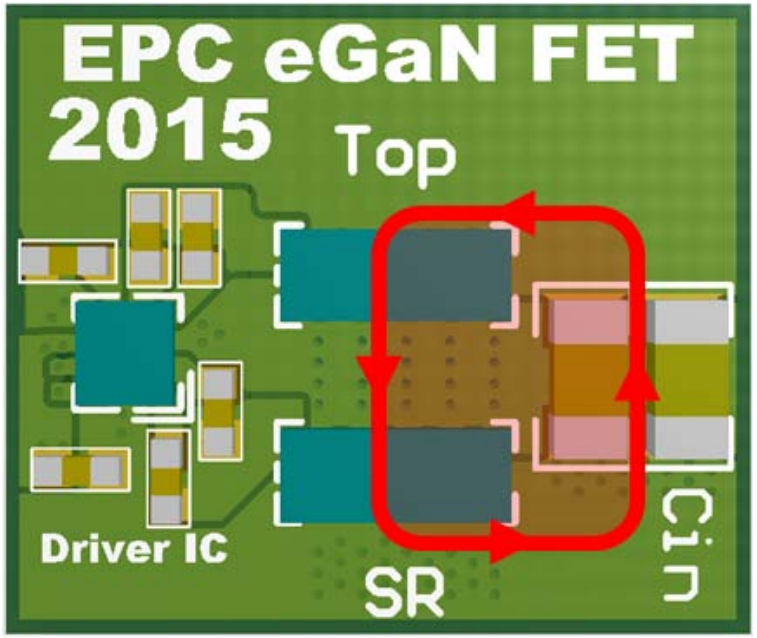
Switching Node Voltage

V_{IN}=12 V V_{OUT}=1.2 V I_{OUT}=20 A

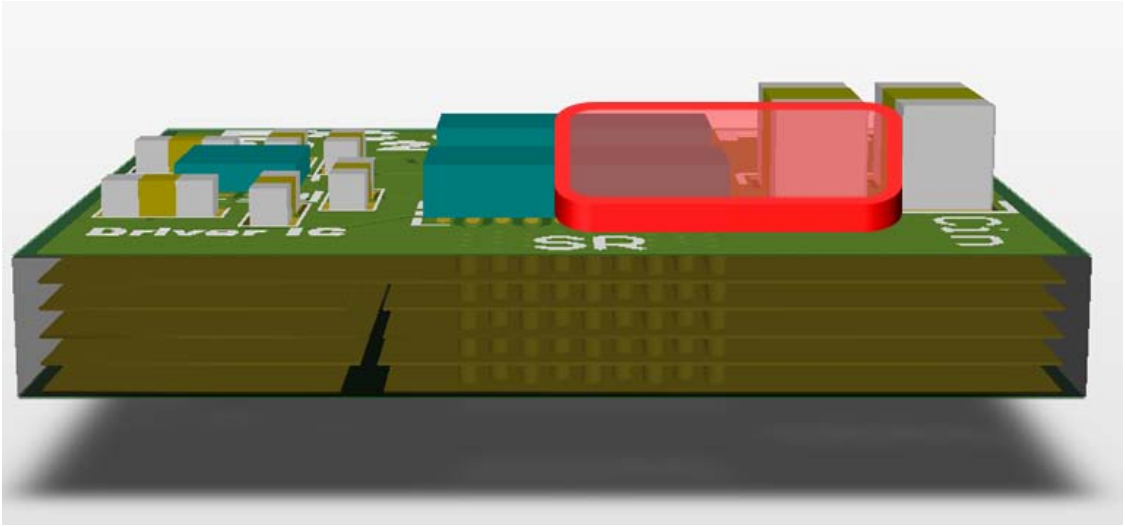
F_S=1 MHz L=150 nH

Conventional Lateral Layout

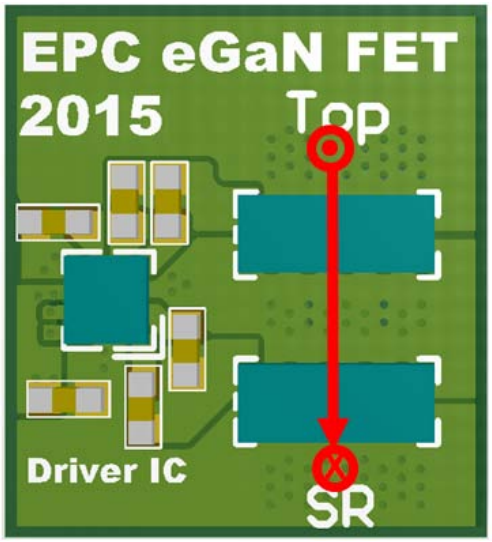
Top View



Side View

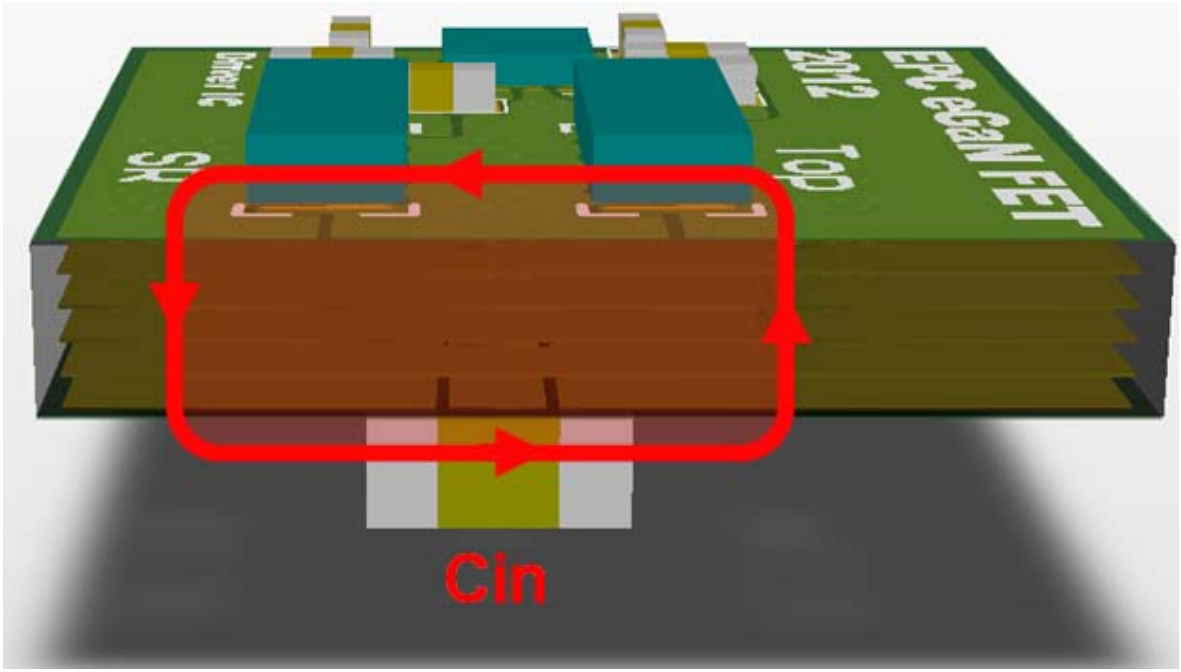


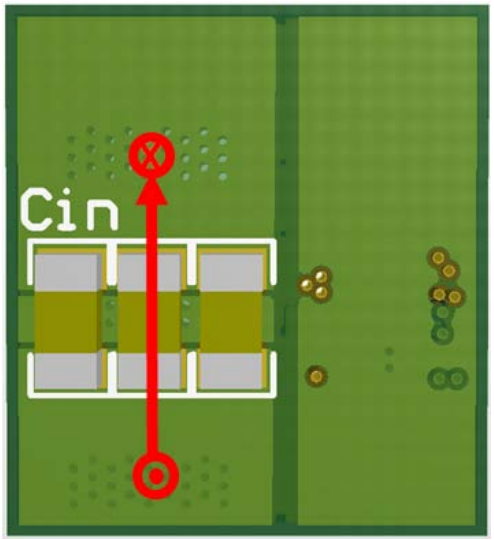
Conventional Vertical Layout



Top View

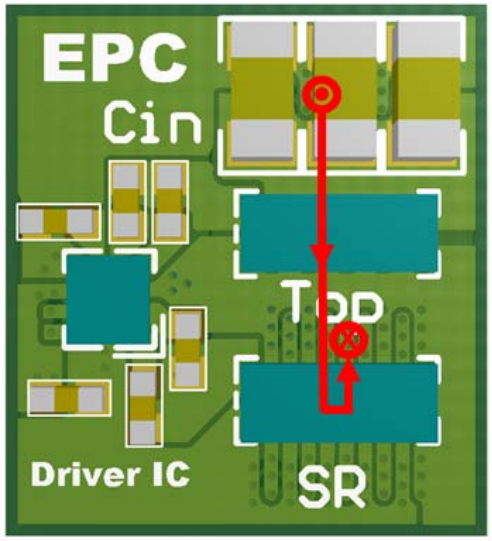
Side View





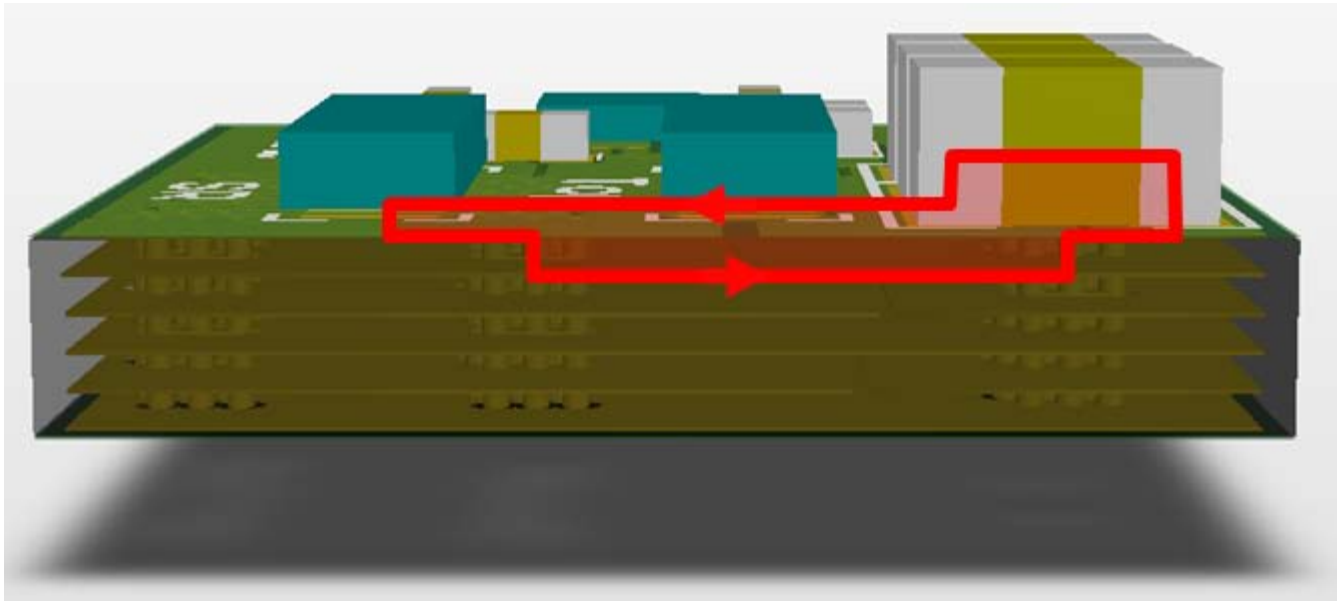
Bottom View

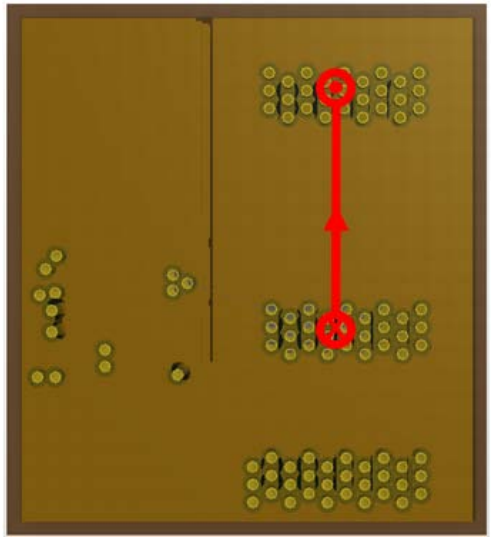
Proposed Optimal Layout



Top View

Side View



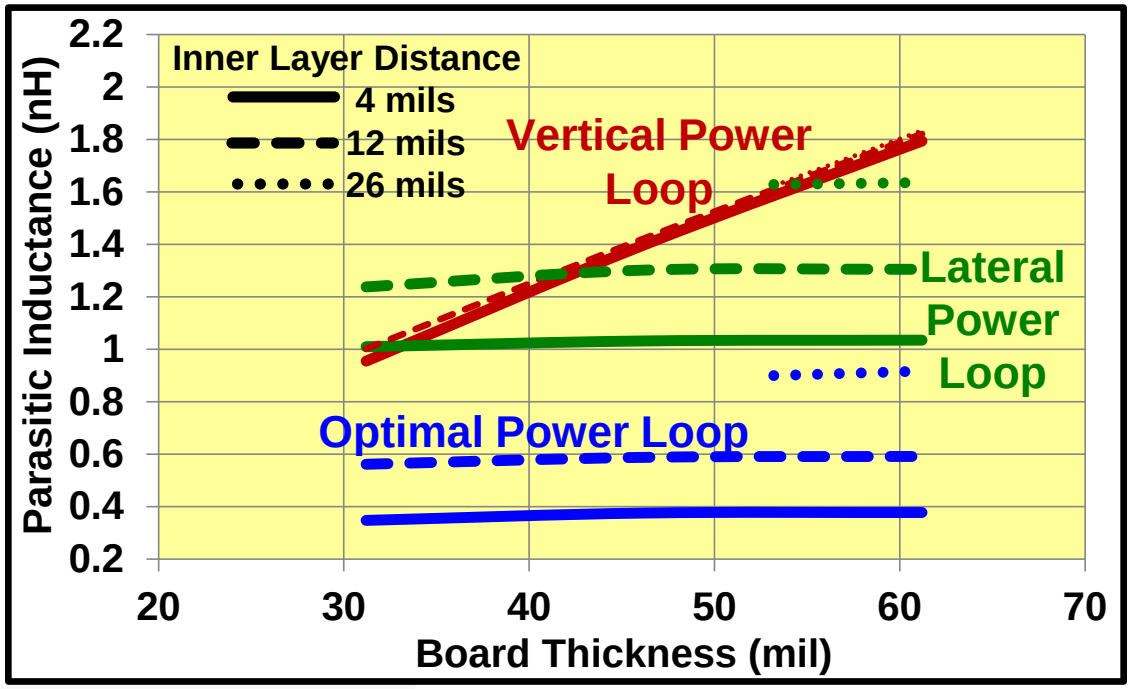


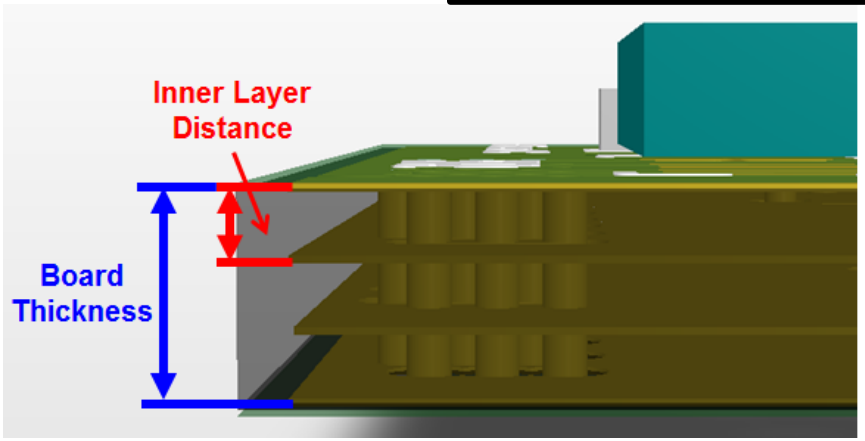
Top View
Inner Layer 1

Layout Comparisons

	Lateral Loop	Vertical Loop	Optimal Loop
Single Sided PCB Capability	Yes	No	Yes
Field Self Cancellation	No	Yes	Yes
Inductance Independent of Board Thickness	Yes	No	Yes
Shield Layer Required	Yes	No	No

Layout Inductance Comparison

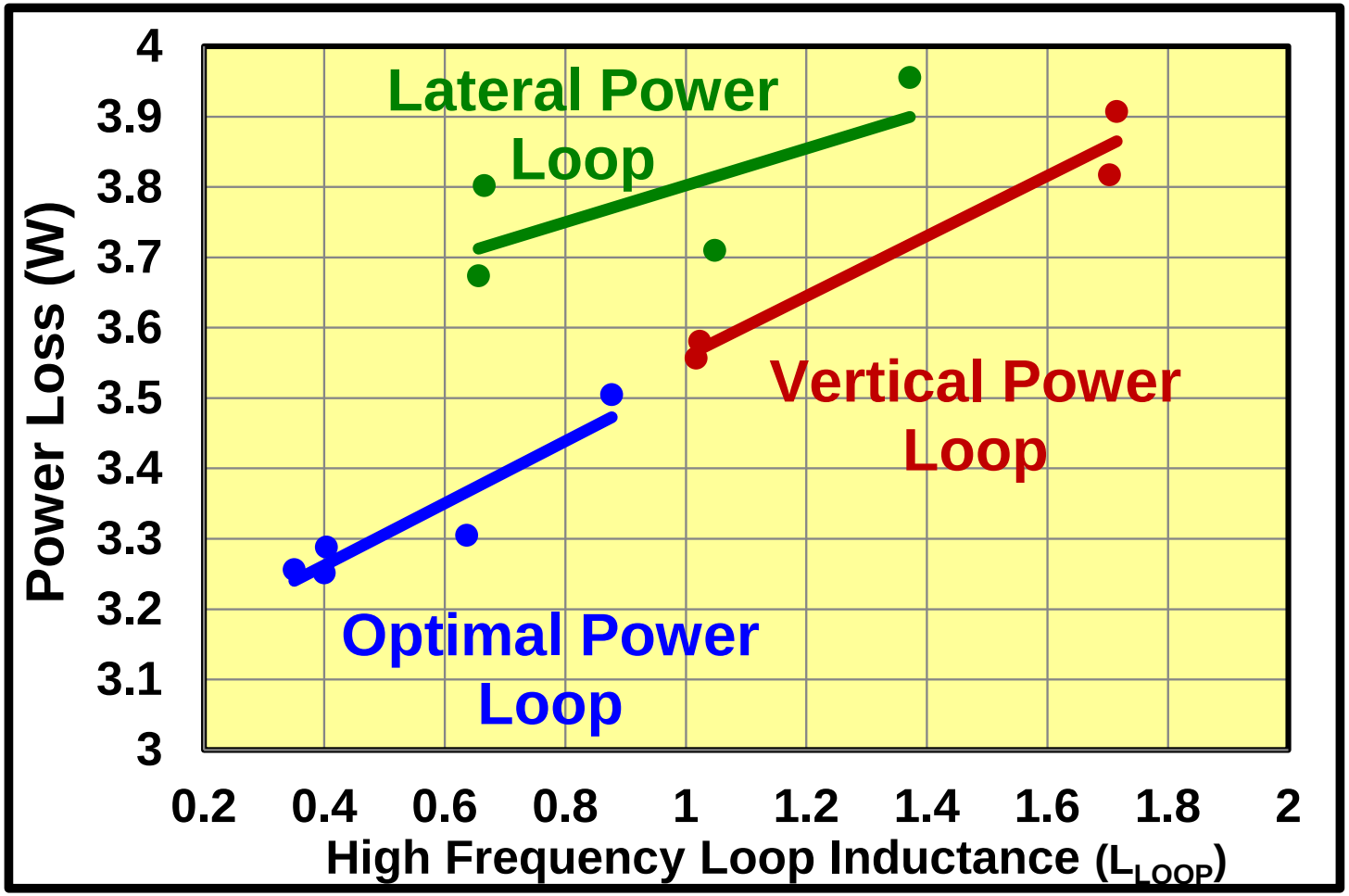




Test Cases

	Board Thickness (mils)	Inner Layer Distance (mils)
Design 1	31	4
Design 2	31	12
Design 3	62	4
Design 4	62	26

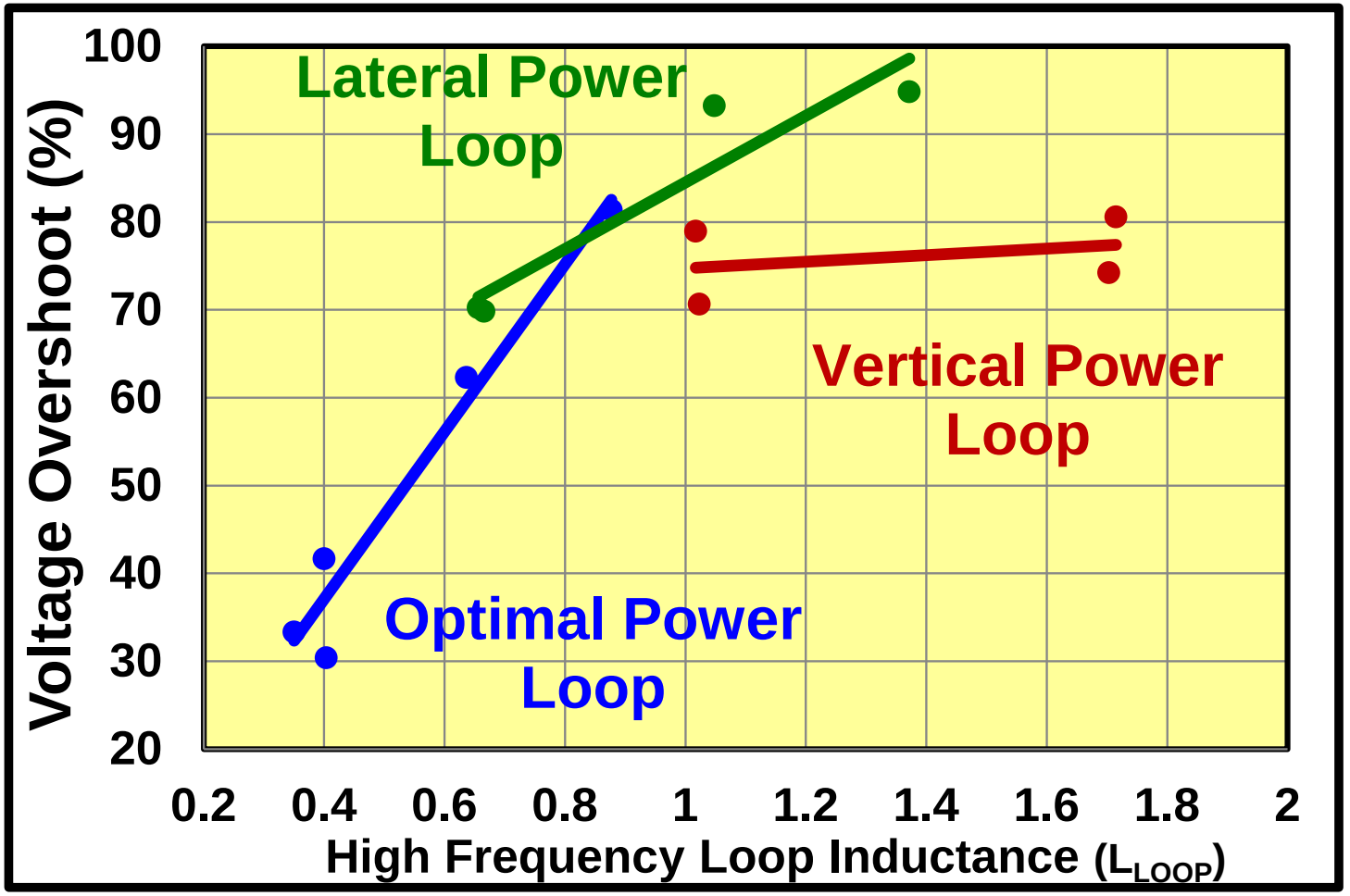
Power Loss Comparison



V_{IN}=12 V V_{OUT}=1.2 V I_{OUT}=20 A F_S=1 MHz L=300 nH

T/SR: EPC2015 Driver LM5113

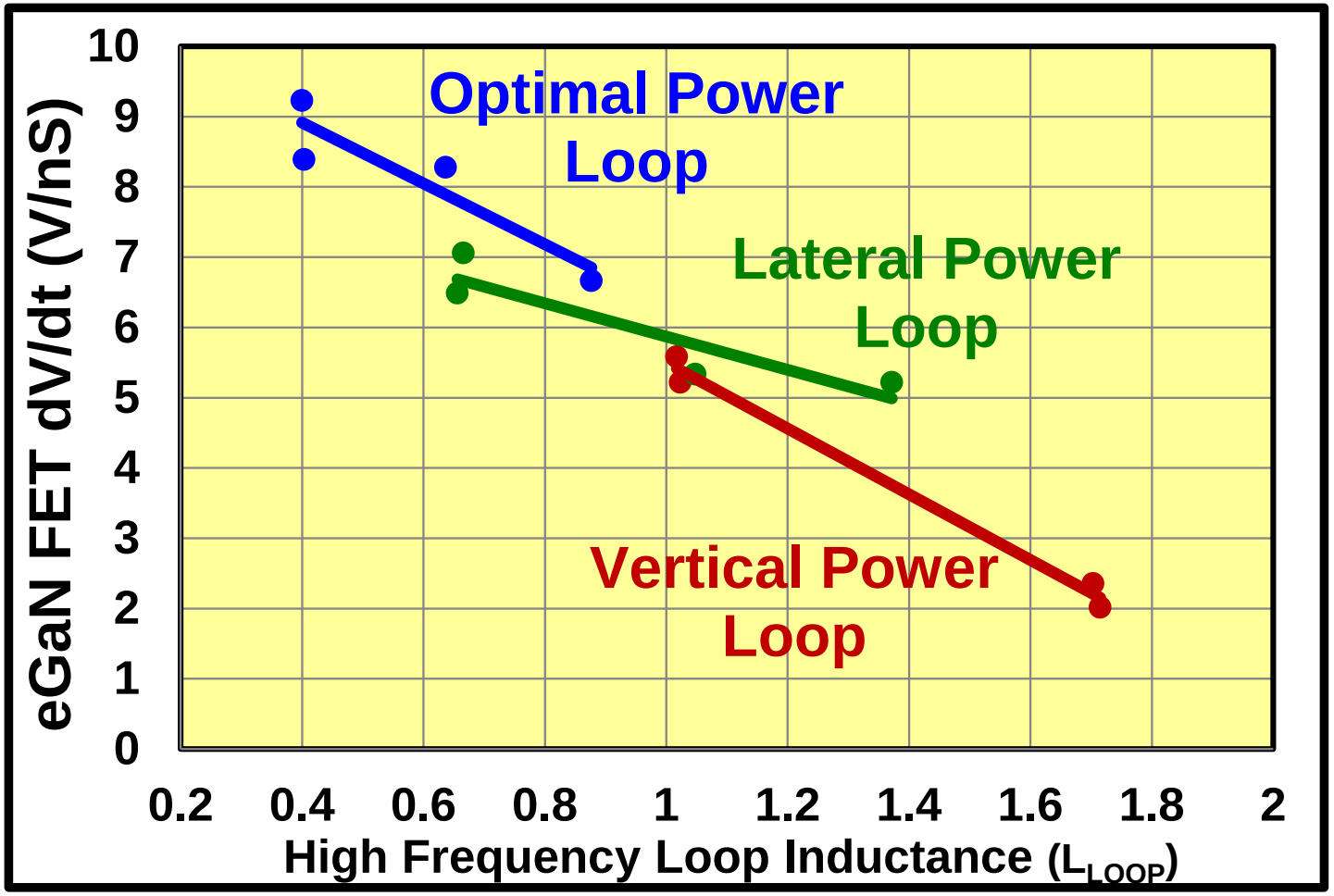
Voltage Overshoot Comparison



V_{IN}=12 V V_{OUT}=1.2 V I_{OUT}=20 A F_S=1 MHz L=300 nH

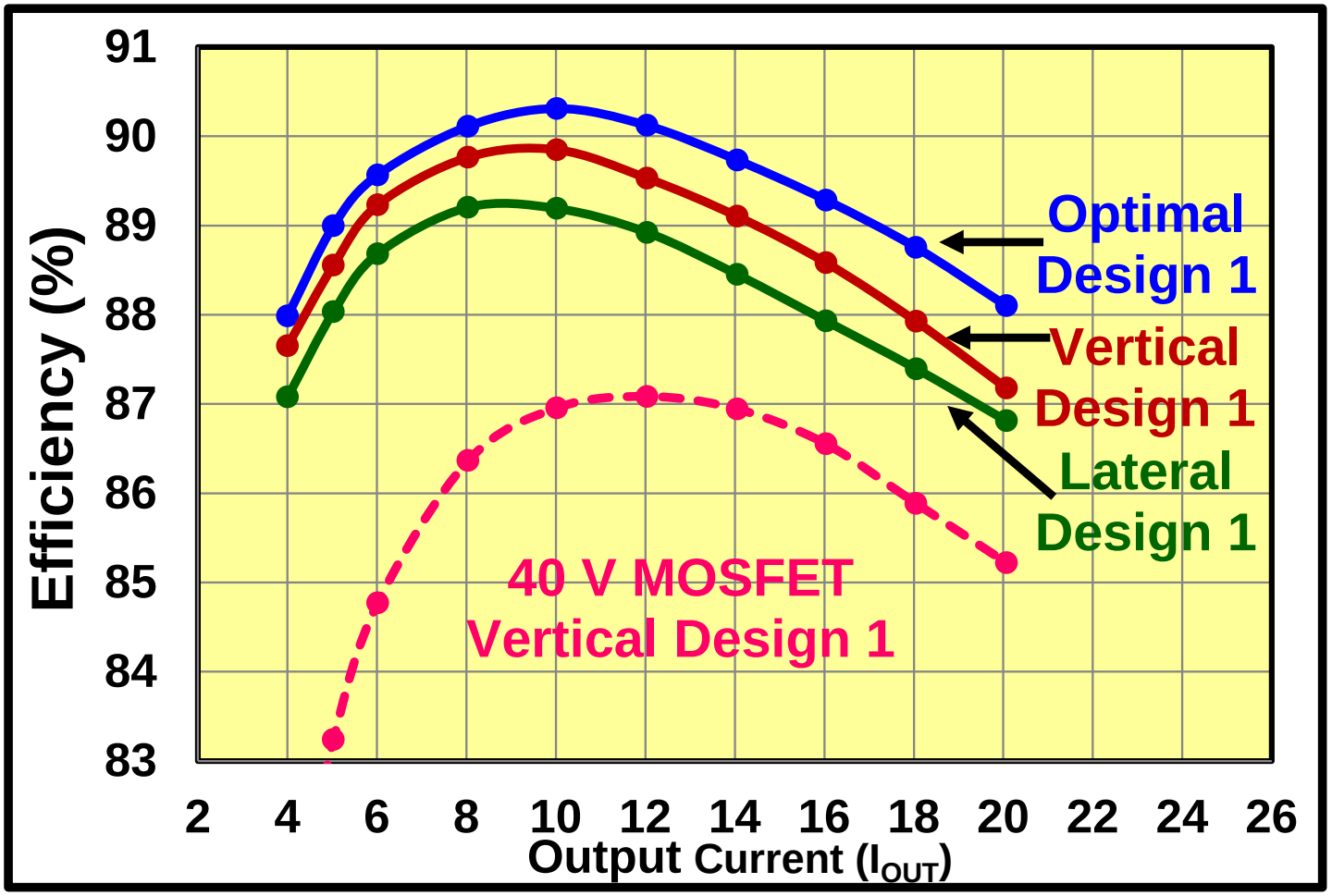
T/SR: EPC2015 Driver LM5113

Switching Speed Comparison



V_{IN}=12 V V_{OUT}=1.2 V I_{OUT}=20 A F_S=1 MHz L=300 nH
T/SR: EPC2015 Driver LM5113

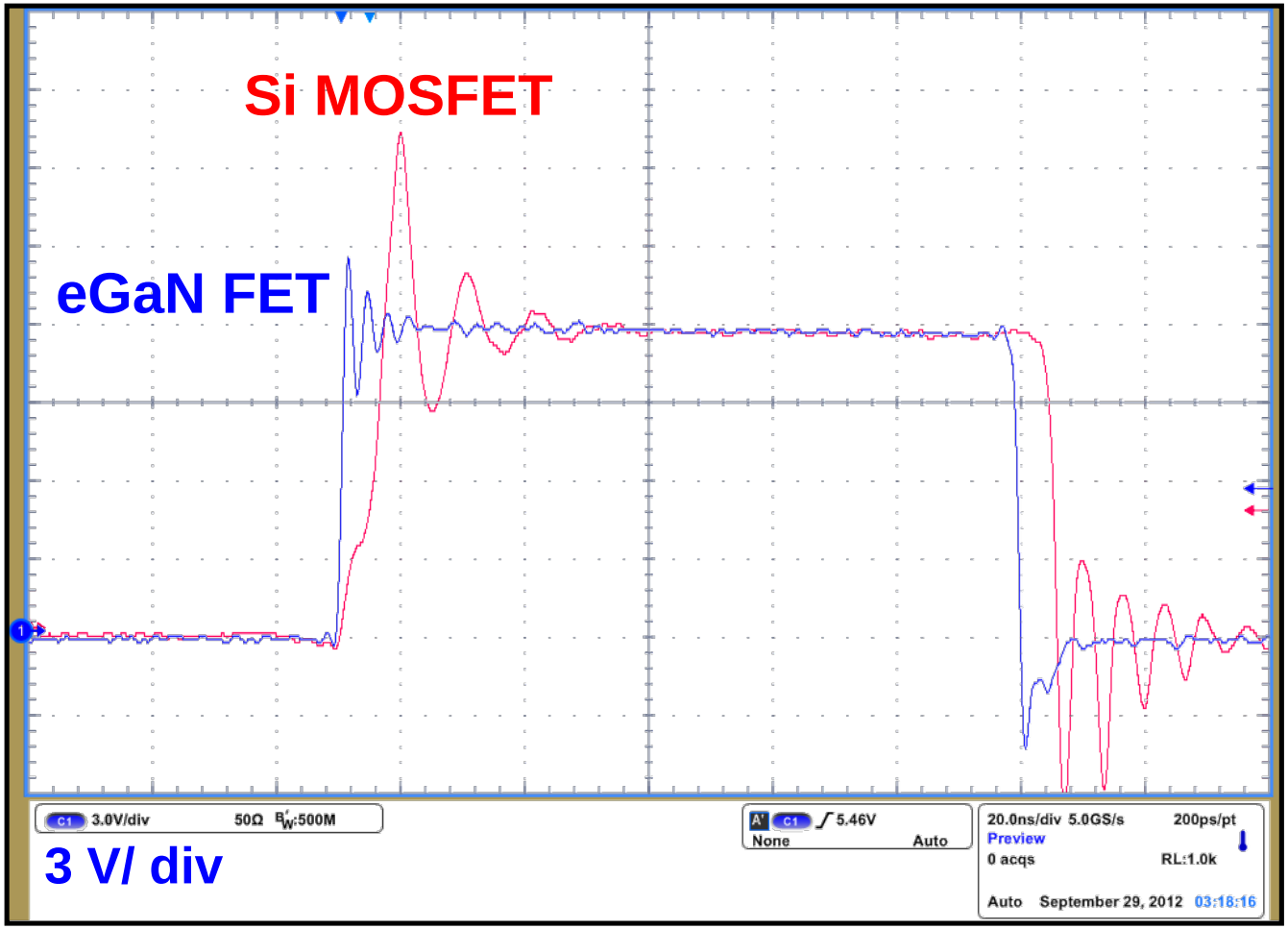
Efficiency Comparison



V_{IN}=12 V V_{OUT}=1.2 V F_S=1 MHz L=300 nH

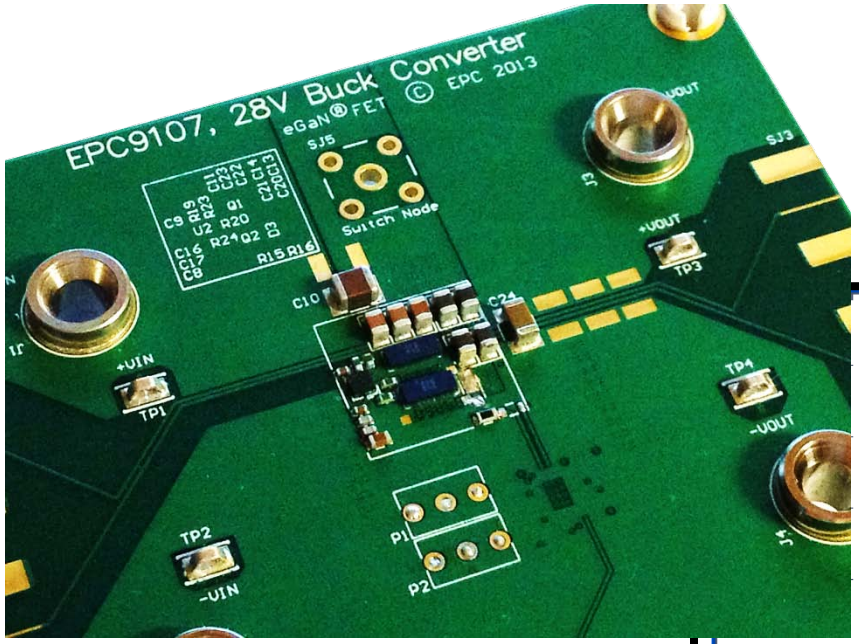
GaN T/SR: EPC2015 Driver LM5113

eGaN FET vs. MOSFET

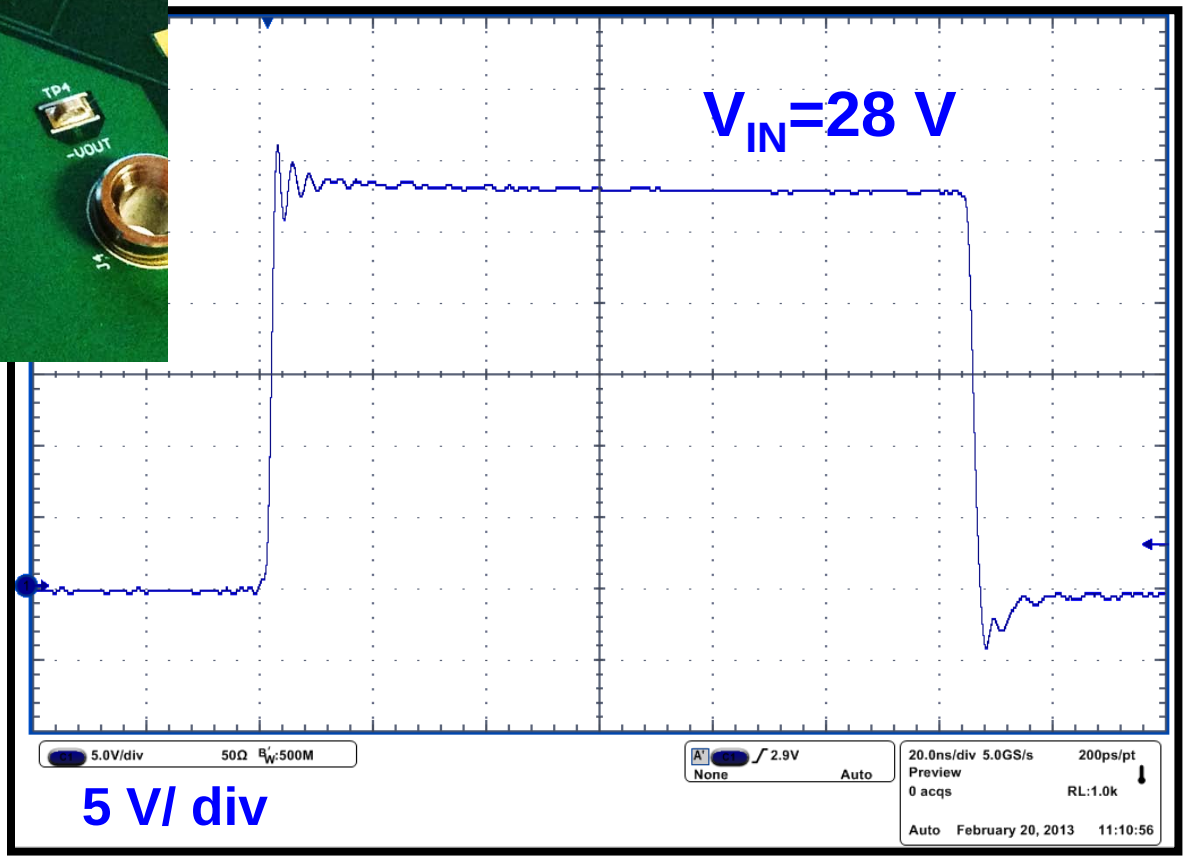


V_{IN}=12 V V_{OUT}=1.2 V I_{OUT}=20 A F_S=1 MHz L=300 nH eGaN FET
T/SR: EPC2015 MOSFET T:BSZ097N04 SR:BSZ040N04

EPC9107 Demonstration Board



V_{IN}=12-28 V V_{OUT}=3.3 V
I_{OUT}=15 A F_S=1 MHz
2 x EPC2015



Switching Node Voltage

V_{IN}=28 V I_{OUT}=15 A

Summary

eGaN FETs improve performance in high switching frequency converters:

- **Lower FOM (Q_{GD}+Q_{GS2})*R_{DSON}**
- **Lower Package Parasitics**
- **PCB Layout Limits Performance**
- **Optimizing Layout Enhances Performance**

EPC
EFFICIENT POWER CONVERSION

The end of the road for silicon…..

is the beginning of the eGaN FET journey!